



#27 / Appeal
Brief
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KS

Docket No.: M4065.0335/P335-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Howard E. Rhodes

Application No.: 09/318,159

Filed: May 25, 1999

For: TRENCH ISOLATION FOR
SEMICONDUCTOR DEVICES

Group Art Unit: 28

Examiner: G. Munson

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APPELLANT'S BRIEF ON APPEAL

Commissioner for Patents
Washington, DC 20231

Sir:

This is an appeal brief (the "Brief") pursuant to 35 U.S.C. § 134 and 37 C.F.R. §§ 1.191 et seq. from the final rejection of claims 45, 46, 49-52, 54-57, 59, 60 and 68-76 of the above-identified application (the "Application") mailed August 7, 2001. The Notice of Appeal was filed on December 7, 2001. The fees for submitting this Brief (\$320.00, 37 C.F.R. § 1.17(c)) and for one month extension of time are attached hereto. Any deficiency in the fees associated with this Brief should be charged to our Deposit Account No. 04-1073. Enclosed are an original and two copies of this Brief with appended claims.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Micron Technology, Inc., a Corporation of the State of Delaware, the assignee of this application.

II. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences known to Appellant, his legal representative or the assignee that will directly affect or be directly affected by, or have a bearing on, the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 43, 44, 48, 53 and 58 of the above-referenced application have been cancelled. (June 13, 2000 Amendment). New claims 68-76 have been added. (June 13, 2000 Amendment). No claims have been allowed. The claims on appeal are claims 45, 46, 49-52, 54-57, 59, 60 and 68-76.

Claims 72 and 76 stand rejected under 35 U.S.C. § 112, first paragraph, as containing new matter.

Claims 45, 46, 49-52, 54-57, 59, 60, 68-70, 72-74 and 76 stand rejected under 35 U.S.C. § 103 as being unpatentable over Schuegraf et al. (U.S. Patent No. 5,702,976) in view of Jeng et al. (U.S. Patent No. 5,492,853).

Claims 45, 46, 49-52, 54-57, 59, 60, 68-71 and 73-75 stand rejected under 35 U.S.C. § 102 as being anticipated by either Jeng (U.S. Patent No. 5,706,164) or Narita (U.S. Patent No. 5,859,451).

Claims 46, 49-52, 54, 55, 57, 59, 60, 68-71 and 73-75 stand rejected under 35 U.S.C. § 102 as being anticipated by Kohara et al. (U.S. Patent No. 4,799,093).

Claims 45, 49-52 and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Kooi et al. (U.S. Patent No. 3,755,001).

Claims 45, 49-52 and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Doo (U.S. Patent No. 3,386,865).

Claims 49-52 and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Mastroianni et al. (U.S. Patent No. 4,443,932).

Claims 45, 49-52 and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Custode et al. (U.S. Patent No. 4,990,983).

Claims 46, 49-52, 54, 55, 57, 59, 60, 68-71 and 73-75 stand rejected under 35 U.S.C. § 102 as being anticipated by Joo et al. (U.S. Patent No. 5,841,163).

IV. STATUS OF AMENDMENTS

No amendments have been submitted subsequent to the final Office Action dated August 7, 2001 ("final Office Action").

V. SUMMARY OF INVENTION

The claimed invention relates to integrated circuit structures having active regions separated by isolation trenches comprising two dielectric materials. According to the claimed invention, the isolation trench is formed by "partially filling the trench with a dielectric material so that at least the sidewalls of the trench are coated with the dielectric material." (Application at 3, lines 10-12; Figures 3-5). After ion implantation below the isolation trench, "the remainder of the trench can be filled with the same or another dielectric material." (Application at 3, lines 20-21; Figures 7-8). In this manner, the dielectric material which partially fills the trench "can serve as a mask so that substantially all of the ions implanted below the isolation trenches are displaced from the active regions." (Application at 3, lines 16-19). This way, "an implanted ion profile can be obtained so that the implanted ions are displaced from the sidewalls of the trench 22 by a distance equal to the sidewall thickness of the dielectric layer 24." (Application at 7, lines 27-30; Figure 4).

VI. ISSUES

Whether the rejection of claims 72 and 76 under 35 U.S.C. § 112, first paragraph, as containing new matter should be reversed.

Whether the rejection of claims 45, 46, 49-52, 54-57, 59, 60, 68-70, 72-74 and 76 under 35 U.S.C. § 103 as being unpatentable over Schuegraf et al. (U.S. Patent No. 5,702,976) in view of Jeng et al. (U.S. Patent No. 5,492,853) should be reversed.

Whether the rejection of claims 45, 46, 49-52, 54-57, 59, 60, 68-71 and 73-75 under 35 U.S.C. § 102 as being anticipated by either Jeng (U.S. Patent No. 5,706,164) or Narita (U.S. Patent No. 5,859,451) should be reversed.

Whether the rejection of claims 46, 49-52, 54, 55, 57, 59, 60, 68-71 and 73-75 under 35 U.S.C. § 102 as being anticipated by Kohara et al. (U.S. Patent No. 4,799,093) should be reversed.

Whether the rejection of claims 45, 49-52 and 68-71 under 35 U.S.C. § 102 as being anticipated by Kooi et al. (U.S. Patent No. 3,755,001) should be reversed.

Whether the rejection of claims 45, 49-52 and 68-71 under 35 U.S.C. § 102 as being anticipated by Doo (U.S. Patent No. 3,386,865) should be reversed.

Whether the rejection of claims 49-52 and 68-71 under 35 U.S.C. § 102 as being anticipated by Mastroianni et al. (U.S. Patent No. 4,443,932).

Whether the rejection of claims 45, 49-52 and 68-71 under 35 U.S.C. § 102 as being anticipated by Custode et al. (U.S. Patent No. 4,990,983) should be reversed.

Whether the rejection of claims 46, 49-52, 54, 55, 57, 59, 60, 68-71 and 73-75 under 35 U.S.C. § 102 as being anticipated by Joo et al. (U.S. Patent No. 5,841,163) should be reversed.

VII. GROUPING OF CLAIMS

None of the claims in the appeal stand or fall together. The reasons why Appellant believes the claims to be separately patentably are set forth in the Argument section of this Brief in compliance with M.P.E.P. § 1206.

VIII. ARGUMENTS

A. CLAIMS 72 AND 76 ARE IN FULL COMPLIANCE WITH 35 U.S.C. § 112, FIRST PARAGRAPH

Claims 72 and 76 stand rejected under 35 U.S.C. § 112, first paragraph, as containing new matter.

Claims 72 and 76 depend on independent claims 68 and 73, respectively, which recite an integrated circuit (claim 68) and a memory device (claim 73) comprising “a field isolation region” separating “a plurality of active regions” and including “an isolation trench.” Independent claims 68 and 73 further recite that the isolation trench includes “a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls,” as well as “an ion implanted region of said semiconductor substrate below said second area, substantially all ions from said ion implanted region being displaced away from” the active regions. Claims 72 and 76 further recite that the first and second dielectric materials “are different.”

Appellant respectfully submits that the specification satisfies the written description requirement of 35 U.S.C. § 112, first paragraph, and that, consequently, the subject matter of claims 72 and 76 does not contain new matter.

According to Federal Circuit case law, “the disclosure need only reasonably convey to persons skilled in the art that the inventor had possession of the subject matter in

question.” See Fujikawa v. Wattanasin, 93 F.3d 1559, 1570 (Fed. Cir. 1996); See also In re Alton, 76 F.3d 1168, 1175 (Fed. Cir. 1996) (“If a person of ordinary skill in the art would have understood the inventor to have been in possession of the claimed invention at the time of filing, even if every nuance of the claim is not explicitly described in the specification, then the adequate written description requirement is met.”); Monsanto Co. v. Mycogen Plant Science, Inc., 61 F. Supp. 2d 133, 188 (D. Del. 1999) (“The applicant need not describe the subject matter claimed in exact terms.”); See also Ralston Purina Co. v. Far-Mar-Co., 772 F.2d 1570, 1575 (Fed. Cir. 1985); Plastic Container Corp. v. Continental Plastics of Oklahoma, Inc., 607 F.2d 885, 886 (10th Cir. 1979).

More importantly, “[T]he law . . . ^{however} does not require . . . ^{such} an example to satisfy the written description requirement.” Flehmig v. Giesa, 13 U.S.P.Q.2d 1052 (Bd. Pat. App. & Int’f 1989). In fact, “it is not essential to *name* the claimed compounds, and . . . preference for the claimed compounds is not necessarily a requirement.” Flynn v. Eardley, 479 F.2d 1393, 1395, 178 U.S.P.Q. 288, 289 (CCPA 1973) (emphasis added). For example, the court in Bigham v. Godtfredsen reasoned that “[T]he generic term ‘halogen’ comprehends a limited number of species” and, accordingly, the Court concluded that the term “halogen” “ordinarily constitutes a sufficient written description of the common halogen species.” Bigham v. Godtfredsen, 857 F.2d 1415, 1417 (Fed. Cir. 1988).

In the present case, the specification of the present Application does not limit the dielectric material to silicon oxide, and it is clear that a variety of other “suitable” dielectric materials could also be used. For example, the “Summary” part of the Application clearly specifies that “[A]fter the ions are implanted . . . the remainder of the trench can be filled with the same or *another* dielectric material.” (Application at 3, lines 19-21; emphasis added). The “Description” part of the Application further notes that “the trenches 22 are only partially filled with an oxide or other dielectric 24” (Application at 7, lines 22-24) and that “[S]uitable dielectric materials include oxides *such as* silicon oxide (SiO₂).” (Application at 6, lines 22-24; emphasis added). According to an alternative embodiment of the invention, “an oxide or other dielectric layer 24A with poor conformal property

partially fills the trenches 22.” (Application at 9, lines 11-13; Figure 5). Subsequent to partially filling of trenches 22, another dielectric material such as “a CVD oxide 34 is deposited to fill the trenches completely.” (Application at 9, lines 32-33; Figure 6).

Accordingly, in view of Flehmg and Bigham, the disclosure in the present Application of silicon dioxide as a first dielectric, followed by the disclosure of “another dielectric material” (i.e., a dielectric material other than silicon dioxide) satisfies the reasonable conveyance test articulated by courts. The assertion in the final Office Action that “the identity of the other dielectric material must be clearly disclosed rather than kept secret” (Office Action at 6) is a clear misunderstanding and misinterpretation of the law. The law does not require a particular example to satisfy the requirements of the 35 U.S.C. § 112, first paragraph. The subject matter of claims 72 and 76 is disclosed in the specification and it is not new matter. In view of the above, Appellant respectfully requests reversal of the rejection of claims 72 and 76.

45, 46, 72, 76 B. CLAIMS 45, 46, 49-52, 54-57, 59, 60, 68-70, 72-74 AND 76 ARE PATENTABLE OVER SCHUEGRAF ET AL. (U.S. PATENT NO. 5,702,976) AND JENG ET AL. (U.S. PATENT NO. 5,492,853)

Claims 45, 46, 49-52, 54-57, 59, 60, 68-70, 72-74 and 76 stand rejected under 35 U.S.C. § 103 as being unpatentable over Schuegraf et al. (U.S. Patent No. 5,702,976) (“Schuegraf”) in view of Jeng et al. (U.S. Patent No. 5,492,853) (“Jeng ‘853”). The final Office Action asserts that the claimed first dielectric material reads on dielectric film 24 of Figure 3D of Schuegraf and that the claimed second dielectric material reads on dielectric material 26 of the same Figure. (Office Action at 3). The Office Action also asserts that “[I]mpurity dopants in substrate are conventional, as applicant would agree and as shown by Jeng et al (column 3, line 61, P-substrate), which would have been obvious to use for substrate 10 of Schuegraf et al (Figure 3D).” (Office Action at 3). Thus, the Office Action

concludes that the claimed ions do not distinguish over the ions in the doped substrate 10 of Schuegraf. (Office Action at 3).

As noted above, the claimed invention relates to isolation trenches formed of two dielectric materials. As such, independent claims 68 and 73 recite an integrated circuit and a memory device, respectively, comprising “a field isolation region” separating “a plurality of active regions” and including “an isolation trench.” Independent claims 68 and 73 further recite that the isolation trench includes “a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls.” Independent claims 68 and 73 also recite “an ion implanted region of said semiconductor substrate below said second area, substantially all ions from said ion implanted region being displaced away from said active regions.” The first and second dielectric materials are “the same” (claims 71, 75) or “different” (claims 72, 76).

Dependent claims 49 and 57 recite that “the implanted ions have a conductivity type the same as the substrate,” while dependent claims 50 and 54 recite that “the implanted ions establish a field threshold voltage.” Dependent claims 69 and 74 further recite that the first area “also includes said first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom.” The ions are implanted into the substrate and below the first area “to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material” (claims 51, 59) or “to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material” (claims 52, 60). Dependent claim 55 also recites that “the sidewall thickness of said first area filled with said first dielectric material is less than about forty percent the width of the isolation region,” while dependent claim 56 recites that “the first dielectric material has a sidewall thickness of at least about one hundred angstroms.”

Schuegraf relates to “a trench isolation process which alleviates the problem of void formation during dielectric refill.” (Col. 2, lines 49-51). According to Schuegraf,

“recesses (22) preferably having a trench profile” are formed by removing portions of a semiconductor substrate 10. (Col. 2, lines 60-61; Figure 3A). Schuegraf teaches that “[T]he trenches (22) are then refilled with a material (26) having a dielectric constant lower than the dielectric constant of silicon dioxide.” (Col. 2, lines 61-63; Figure 3D). To avoid contamination of substrate regions adjacent to trenches 22, Schuegraf further teaches that “it is preferably to form a barrier layer 24 over the trenches 22 prior to dielectric refill.” (Col. 5, lines 9-12; Figure 3B). In this manner, by “utilizing dielectric materials having a lower dielectric constant that used in the prior art,” the shallow trench isolation of Schuegraf “maintains effective device isolation.” (Col. 4, lines 37-40).

Jeng `853 relates to the formation of a trench and insulating layer as part of a “process for forming a contact to a semiconductor substrate on a semiconductor device.” (Abstract). According to Jeng `853, “[T]he trench comprises a bottom (30) and a first sidewall (32) consisting of silicon and a second sidewall (34) comprising field oxide.” (Col. 2, lines 1-2; Figure 3). After the formation of a protective layer 52 over the first and second sidewalls 32, 34, Jeng `853 teaches that “[T]he trench bottom (30) is oxidized to form a layer of oxide (54) over the bottom of the trench, thereby insulating the trench bottom, the layer of oxide (54) contacting the second sidewall (34).” (Col. 2, lines 4-7; Figure 5). Subsequent to the removal of the protective layer 54 and the exposure of the sidewalls 32, 34, “[A] conductive layer (60) is formed over the exposed trench sidewalls, the trench bottom being insulated from the conductive layer by the oxide on the trench bottom.” (Col. 2, lines 9-12; Figure 6).

The subject matter of claims 45, 46, 49-52, 54-57, 59, 60, 68-70, 72-74 and 76 would not have been obvious over Schuegraf and Jeng `853. Indeed, the final Office Action failed to establish a *prima facie* case of obviousness.

Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of

success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 U.S.P.Q.2d 1626, 1630 (Fed. Cir. 1996).

In the present case, the final Office Action fails to establish all elements of a showing of a *prima facie* case of obviousness. Specifically, the prior art references fail to teach or suggest all claim limitations. Neither Schuegraf nor Jeng `853 disclose trenches separating “a plurality of *active regions*” and having a first and a second areas filled with corresponding dielectric materials as well as “an ion implanted region . . . below said second area, *substantially all ions from said ion implanted region being displaced away from said active regions*,” as independent claims 68 and 73 recite (emphasis added). Schuegraf discloses trenches which are “refilled with a dielectric material” with low dielectric constant and which may be lined with a barrier layer 24 prior to the dielectric refill. (Col. 3, lines 61-62). However, Schuegraf does not teach or suggest an ion implanted region directly below the second dielectric area, as in the claimed invention. Schuegraf is also silent about any ions from an ion implanted region “being displaced away from” the active regions, as independent claims 68 and 73 recite. In fact, Schuegraf does not even mention the existence of active regions in the “Detailed Description,” or illustrate any such active regions in the “Drawings.”

Similarly, Jeng `853 does not disclose a trench isolation structure with “a first area filled with a first dielectric material . . . and a second area filled with a second dielectric material,” as independent claims 68 and 73 recite. Jeng `853 also fails to disclose an ion implantation directly below the second area with substantially all ions “being displaced away from” the separated active regions, as independent claims 68 and 73 recite. As noted above, Jeng `853 discloses only a trench having an oxide layer 54 (Figure 6) located at the bottom of the trench and a conductive layer 60 (Figure 6) in direct contact with the oxide

layer 54. Jeng `853 is silent about ion displacement from active regions or about first and second dielectric areas filled with first and second dielectric materials.

Schuegraf and Jeng `853, alone or in combination, also fail to teach or suggest the limitations of dependent claims 45, 46, 49-52, 54-57, 59, 60, 69-70, 72, 74 and 76. Schuegraf and Jeng `853 are silent about any conductivity type of the substrate, much less about implanted ions in such substrate having “a conductivity type the same as the substrate,” as dependent claims 49 and 57 recite, or about implanted ions which “establish a field threshold voltage,” as dependent claims 50 and 54 recite. Schuegraf is silent about substrate conductivity type, ion implantation or types of ion implantation. Schuegraf also fails to disclose a field threshold voltage, much less a “field threshold voltage” established by implanted ions, as dependent claims 50 and 54 recite. Similarly, the only reference Jeng `853 makes to substrate conductivity type is the “portion of the P-substrate becoming N-” when diffusion occurs “from the poly of the storage cell to the substrate.” (Col. 3, lines 59-61). Jeng `853 is silent, however, about ions implanted in a substrate or about implanted ions having “a conductivity type the same as the substrate,” as dependent claims 49 and 57 recite, or about ion implanted establishing “a field threshold voltage,” as dependent claims 50 and 54 recite.

Schuegraf and Jeng `853, alone or in combination, also fail to teach or suggest a first area which “also includes said first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom,” as dependent claims 69 and 74 recite. Schuegraf teaches that “[T]he trenches 22 are then refilled with a material 26 having a dielectric constant lower than the dielectric constant of silicon dioxide” (col. 2, lines 61-63; Figure 3D) and that “it is preferably to form a barrier layer 24 over the trenches 22 prior to dielectric refill.” (Col. 5, lines 9-12; Figure 3B). Figure 3B of Schuegraf illustrates, however, the barrier layer 24, which would arguably correspond to the first dielectric material of the claimed invention, is formed over the bottom and sidewalls of trenches 22, and not “provided on a bottom of said isolation trench,” as dependent claims 69 and 74

recite. Similarly, although the oxide layer 54 of Jeng `853 is formed “over the bottom of the trench, thereby insulating the trench bottom” (col. 2, lines 4-7), Jeng `853 teaches that a conductive layer 60 is formed over the trench bottom, and not a dielectric material, as in the claimed invention.

Schuegraf and Jeng `853, alone or in combination, also fail to teach or suggest the recited spacing and ion implant limitations of dependent claims 51, 52, 55, 56, 59 and 60. Schuegraf and Jeng `853 are silent about ions which are “displaced away from said active regions by a distance at least equal to a sidewall thickness of said first area filled with said first dielectric material,” as independent claim 73 recites. Schuegraf and Jeng `853 do not have any discussion of ion implantation below a trench, much less of ions implantation into a substrate and below a first area “to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material” (claims 51, 59) or “to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material” (claims 52, 60). For the reasons above, Schuegraf and Jeng `853 also fail to teach or suggest that “the sidewall thickness of said first area filled with said first dielectric material is less than about forty percent the width of the isolation region” (claim 55) or that “the first dielectric material has a sidewall thickness of at least about one hundred angstroms” (claim 56). Accordingly, there is no teaching or suggestion in either of these two references, either independently or combined, of the claimed subject matter and reversal of the rejection of claims 45, 46, 49-52, 54-57, 59, 60, 68-70, 72-74 and 76 is respectfully requested.

C. CLAIMS 45, 46, 49-52, 54-57, 59, 60, 68-71 AND 73-75 ARE
NOT ANTICIPATED BY JENG (U.S. PATENT NO.
5,706,164) OR NARITA (U.S. PATENT NO. 5,859,451)

Claims 45, 46, 49-52, 54-57, 59, 60, 68-71 and 73-75 stand rejected under 35 U.S.C. § 102 as being anticipated by either Jeng (U.S. Patent No. 5,706,164) (“Jeng `164”) or Narita (U.S. Patent No. 5,859,451). With respect to Figure 12 of Jeng `164, the final Office Action asserts that the claimed first and second dielectric materials read on

subportions of dielectric layer 7 and that the claimed ions read on subportions of P type substrate 1 under dielectric layer 7. (Office Action at 3). With respect to Figure 1 of Narita, the final Office Action notes that the claimed first and second dielectric materials read on subportions of the field oxide 14. (Office Action at 4).

Jeng `164 relates to a method for increasing the surface area of a stacked capacitor by using an elevated trench isolation structure. (Col. 2, lines 19-24). As part of the fabrication of DRAM devices containing stack capacitors, Jeng `164 teaches the formation in the P-type silicon substrate 1 of a shallow trench 6 which is filled with a TEOS oxide 7. (Col. 3, lines 39-51; Figure 3).

Narita relates to “a one-transistor type memory cell having an associated information storage capacitor.” (Col. 2, lines 14-17). According to Narita, “surface 12 of the semiconductor substrate 10 is divided into a number of device formation zones confined by a field oxide 14, which is formed in a LOCOS (local oxidation of silicon) method.” (Col. 3, lines 4-8; Figure 1).

Neither Jeng `164 nor Narita discloses any of the limitations of the claimed invention. Jeng `164 and Narita do not disclose an isolation trench including “a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls,” as independent claims 68 and 73 recite. Jeng `164 and Narita further fail to disclose “an ion implanted region of said semiconductor substrate below said second area, substantially all ions from said ion implanted region being displaced away from said active regions,” as independent claims 68 and 73 also recite. Jeng `164 teaches an elevated trench isolation structure to increase the surface area of a stacked capacitor. (Col. 2, lines 19-24). Jeng `164 does not disclose or even mention an isolation trench as part of a “field isolation region” separating active regions or having two dielectric material areas. The only dielectric material disclosed by Jeng `164 is the TEOS oxide layer 7 which completely fills trench 6. (Col. 3, lines 48-50). In addition, Jeng `164 does not disclose “an ion implanted region below” the second area, with *substantially all* implanted ions being

displaced away from separated active regions, as independent claims 68 and 73 recite. The only mention to ion implantation in Jeng `164 is the doping of polysilicon via ion implantation, as a well-known method. (Col. 3, lines 25-30). As it is obvious from Figure 12 of Jeng `164, however, the subportions of the p-type substrate 1 under the dielectric layer 12 do not contain implanted ions displaced away from separated active regions.

Similarly, the subportions of the field oxide 14 of Figure 1 of Narita are not part of any isolation trench. In fact, Narita is silent about the existence of an isolation trench in a semiconductor substrate. Further, as illustrated in Figures 1-2 of Narita, the subportions of the field oxide 14 are in direct contact with gate electrode (word line) 26, and thus not separating active regions, as independent claims 68 and 73 recite. Moreover, Narita does not disclose first and second areas which are respectively filled with a first and second dielectric material, and with substantially all implanted ions displaced away from the separated active regions, as independent claims 68 and 73 recite.

Jeng `164 and Narita also fail to teach or suggest the limitations of dependent claims 45, 46, 49-52, 54-57, 59, 60, 69-70, 72, 74 and 76. Jeng `164 and Narita are silent about implanted ions in a substrate having “a conductivity type the same as the substrate,” as dependent claims 49 and 57 recite, or about implanted ions which “establish a field threshold voltage,” as dependent claims 50 and 54 recite. Jeng `164 only mentions that the silicon substrate 1 has a P-type conductivity. (Col. 3, line 17). Jeng `164 is silent, however, about ion implantation or types of ion implantation. Jeng `164 also fails to disclose a field threshold voltage, much less a “field threshold voltage” which is established by implanted ions, as dependent claims 50 and 54 recite. Similarly, the only reference Narita makes to substrate conductivity type is “a P-type silicon substrate 10” with “N-type diffusion regions 18 and 20”. (Col. 3, lines 3, 25). Narita is silent, however, about implanted ions having “a conductivity type the same as the substrate,” as dependent claims 49 and 57 recite, or about ion implanted which establish “a field threshold voltage,” as dependent claims 50 and 54 recite.

Jeng `164 and Narita also fail to disclose that the first area “also includes said first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom,” as dependent claims 69 and 74 recite. As noted above, Jeng `164 teaches a shallow trench 6 which is filled with a TEOS oxide 7 (col. 3, lines 39-51; Figure 3). Jeng `164 does not disclose a shallow trench filled with a first and second dielectric materials, much less a shallow trench having a “first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom,” as dependent claims 69 and 74 recite. Narita is also silent about the existence of an isolation trench in a semiconductor substrate, much less about active regions separated by isolation trenches, or about “first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom,” as dependent claims 69 and 74 recite.

Jeng `164 and Narita are further silent about ions which are “displaced away from said active regions by a distance at least equal to a sidewall thickness of said first area filled with said first dielectric material,” as independent claim 73 recites. Neither Jeng `164 nor Narita discusses ion implantation below a trench, much less ion implantation into a substrate and below a first area “to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material” (claims 51, 59) or “to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material” (claims 52, 60). As noted above, Jeng `164 teaches a capacitor trench and not an isolation trench separating active region, and Narita does not even mention a isolation trench. For the reasons above, Jeng `164 and Narita further fail to teach or suggest that “the sidewall thickness of said first area filled with said first dielectric material is less than about forty percent the width of the isolation region” (claim 55) or that “the first dielectric material has a sidewall thickness of at least about one hundred angstroms” (claim 56). Accordingly, the claimed invention is not anticipated by Jeng `164 or Narita under 35 U.S.C. § 102, and reversal of the rejection of claims 45, 46, 49-52, 54-57, 59, 60, 69-70, 72, 74 and 76 is respectfully requested.

D. CLAIMS 46, 49-52, 54, 55, 57, 59, 60, 68-71 AND 73-75 ARE NOT ANTICIPATED BY KOHARA ET AL. (U.S. PATENT NO. 4,799,093)

Claims 46, 49-52, 54, 55, 57, 59, 60, 68-71 and 73-75 stand rejected under 35 U.S.C. § 102 as being anticipated by Kohara et al. (U.S. Patent No. 4,799,093) (“Kohara”). The final Office Action asserts that the claimed first and second dielectric materials read on subportions of oxide layer 2 of Figure 2C of Kohara and that the claimed ion implanted region reads on region 3 adjacent subportions of region 1. (Office Action at 4).

Kohara relates to a method for reducing the surface area of a memory cell by employing a superposed capacitor. (Col. 1, lines 65- 68; Col. 2, lines 1-4). Kohara teaches that “a thick partition oxide layer (2) . . . is formed on a surface of a P-silicon substrate (1) and a p+ -layer (3) having high impurity concentration for preventing turnover of the P-silicon substrate (1) to n-type is also formed on the surface of the P-silicon substrate (1).” (Col. 1, lines 32-38; Figure 2C).

Kohara discloses neither areas filled with dielectric materials nor an ion implanted region formed directly below them and as part of a field isolation region, as independent claims 68 and 73 recite. In Kohara, the oxide layer (2) of Figure 2C does not comprise a first and second areas filled with a first and second dielectric material. In Kohara, the oxide layer (2) is not part of an isolation trench and, thus, the p+ layer (3) cannot be an implanted region formed below an isolation trench, as independent claims 68 and 73 recite.

Kohara also fails to disclose implanted ions in a substrate having “a conductivity type the same as the substrate,” as dependent claims 49 and 57 recite, or implanted ions which “establish a field threshold voltage,” as dependent claims 50 and 54 recite. Kohara fails to disclose a field threshold voltage, much less a “field threshold voltage” established by implanted ions, as dependent claims 50 and 54 recite. Kohara also fails to disclose that

the first area “also includes said first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom,” as dependent claims 69 and 74 recite. As noted above, Kohara does not disclose a shallow trench filled with a first and second dielectric materials, much less a shallow trench having a “first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom,” as dependent claims 69 and 74 recite.

Kohara is silent about the existence of an isolation trench in a semiconductor substrate, much less about active regions separated by isolation trenches, or about “first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom,” as dependent claims 69 and 74 recite. Kohara is further silent about ions which are “displaced away from said active regions by a distance at least equal to a sidewall thickness of said first area filled with said first dielectric material,” as independent claim 73 recites. Kohara fails to discuss ion implantation below a trench, or ion implantation into a substrate and below the first area “to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material” (claims 51, 59) or “to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material” (claims 52, 60). Kohara is also silent about “the sidewall thickness of said first area filled with said first dielectric material” as being “less than about forty percent the width of the isolation region” (claim 55) or “of at least about one hundred angstroms” (claim 56). Accordingly, none of the limitations of the present invention are described or mentioned in Kohara and, thus, the present invention is not anticipated under 35 U.S.C. § 102. Appellant respectfully requests the reversal of the rejection of claims 46, 49-52, 54, 55, 57, 59, 60, 68-71 and 73-75.

E. CLAIMS 45, 49-52 AND 68-71 ARE NOT ANTICIPATED BY
KOOI ET AL. (U.S. PATENT NO. 3,755,001)

Claims 45, 49-52 and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Kooi et al. (U.S. Patent No. 3,755,001) ("Kooi"). The final Office Action asserts that the claimed first and second dielectric materials read on subportions of oxide 5 of Figure 8 or oxide 29 of Figure 10, and that the claimed ion implanted region reads on zone 6 of Figure 8 or zone 28 of Figure 10. (Office Action at 4).

Kooi relates to a method of fabricating semiconductor devices having selective doping and selective oxidation. (Title; Col. 1, lines 4-11). As part of the fabrication of "a target plate (1) for converting electromagnetic radiation into electric signals," Kooi teaches that grooves 4 formed into plate 1 of n-type silicon "are covered with a layer 5 of silicon oxide which at the bottom of the grooves adjoins a surface zone 6 of n-type silicon having higher doping than the region 1." (Col. 6, lines 9-20; Figures 1-2).

Kooi does not disclose an isolation trench or "a second area filled with a second dielectric material" situated within sidewalls of "a first area filled with a first dielectric material," as independent claim 68 recites. Further, Kooi does not disclose "an ion implanted region . . . below said second area," as independent claim 68 further recites. Kooi is also silent about the ion displacement limitation of claim 68, of "substantially all ions from said ion implanted region being displaced away from said separated active regions." As shown in Figures 8 and 10 of Kooi, the ion implanted regions 6 and 28 are in contact with the dielectric materials 5 and 29, respectively, but these dielectric materials are simply not part of an isolation trench, as independent claim 68 recites.

Kooi also fails to teach or suggest implanted ions in a substrate having "a conductivity type the same as the substrate," as dependent claim 49 recites, or implanted ions which "establish a field threshold voltage," as dependent claim 50 recites. Kooi only mentions that plate 1 is of n-type silicon. (Col. 6, line 12). Kooi is silent, however, about ion implantation or types of ion implantation. Kooi also fails to disclose a field threshold

voltage, much less a “field threshold voltage” established by implanted ions, as dependent claim 50 recites. Kooi also fails to discuss ion implantation below a trench, much less ion implantation into a substrate and below a first area “to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material” (claim 51) or “to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material” (claim 52). Accordingly, the subject matter of claims 45, 49-52 and 68-71 is not anticipated by Kooi, and Appellant respectfully requests the reversal of the rejection of these claims.

F. **CLAIMS 45, 49-52 AND 68-71 ARE NOT ANTICIPATED BY
DOO (U.S. PATENT NO. 3,386,865)**

Claims 45, 49-52, and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Doo (U.S. Patent No. 3,386,865) (“Doo”). The final Office Action asserts that, with respect to Figures 5 and 6 of Doo, the claimed first and second dielectric materials read on subportions of oxide 6, and that the claimed ion implanted region “comprises region 9.” (Office Action at 4).

Doo relates to a method of making planar semiconductor devices isolated by encapsulating oxide filled channels. (Title; Col. 1, lines 22-26). As such, Doo discloses “isolating channels of the encapsulating SiO₂(6)” below which “p+ regions of semiconductor material (9)” are disposed (Col. 3, lines 64-75), to provide heat dissipation. (Col. 5, line 21). Thus, by providing “a combination of PN junction and encapsulant isolation,” Doo achieves a “superior structure . . . which permits a high density of devices on a substrate and the reduced deleterious effects of the oxide type of the encapsulant isolation.” (Col. 5, lines 17-25).

Doo does not disclose an isolation trench with a first and second areas filled with a first and second dielectric material, or “an ion implanted region” with ions which are displaced away from separated active regions, as independent claim 68 recites. In Figures 5 and 6 of Doo, the p+ region 9 is in contact with the SiO₂ filled channel 6, but such SiO₂

filled channel is not part of an isolation trench, as independent claim 68 recites. Further, Doo is also silent about ion displacement, which is a limitation of claim 68 of “substantially all ions from said ion implanted region being displaced away from said separated active regions.” Doo only refers to “a portion of a substrate 1 of semiconductor material of a first conductivity type labelled (sic) arbitrarily P” and to a “region of higher conductivity type 4 labelled (sic) P+.” (Col. 2, lines 21-30).

Doo also fails to teach or suggest implanted ions in a substrate which “establish a field threshold voltage,” as dependent claim 50 recites. Doo only mentions that substrate 1 is “labelled (sic) arbitrarily P” and that region 4 has a higher conductivity. (Col. 2, lines 21-30). Doo is silent, however, about ion implantation or type of ion implantation. Doo also fails to disclose a field threshold voltage, much less a “field threshold voltage” established by implanted ions, as dependent claim 50 recites. Doo also fails to discuss ion implantation below a trench, much less ion implantation into a substrate and below a first area of such substrate “to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material” (claim 51) or “to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material” (claim 52). Accordingly, the subject matter of claims 45, 49-52 and 68-71 is not anticipated by Doo and Appellant respectfully requests the reversal of the rejection of claims 45, 49-52 and 68-71.

G. CLAIMS 45, 49-52 AND 68-71 ARE NOT ANTICIPATED BY
MASTROIANNI ET AL. (U.S. PATENT NO. 4,443,932)

Claims 49-52 and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Mastroianni et al. (U.S. Patent No. 4,443,932) (“Mastroianni”). The final Office Action asserts that the claimed first and second dielectric materials read on subportions of isolation region 125 of Figure 3J and that the claimed ion implanted region reads on a subportion of channel stop region 102 of Figure 3J. (Office Action at 5).

Mastroianni relates to self-aligned semiconductor devices which are fabricated “using two sets of superposed pattern forming layers; a master mask layer containing the self-aligned patterns, and a pattern selector layer set which allows different apertures in the master mask layer to be selectively re-opened so that different device regions may be sequentially formed.” (Abstract).

Mastroianni does not disclose an isolation trench or “a second area filled with a second dielectric material” situated within sidewalls of “a first area filled with a first dielectric material,” as independent claim 68 recites. Further, Mastroianni does not disclose “an ion implanted region . . . below said second area,” as independent claim 68 also recites. Figure 3J of Mastroianni does not show or suggest “a second area filled with a second dielectric material” situated within the sidewalls of “a first area filled with a first dielectric material” or “an ion implanted region . . . below said second area,” as independent claim 68 recites. Mastroianni is also silent about ion displacement, which is a limitation of claim 68 of “substantially all ions from said ion implanted region being displaced away from said separated active regions.”

Mastroianni also fails to teach or suggest implanted ions in a substrate having “a conductivity type the same as the substrate,” as dependent claim 49 recites, or implanted ions which “establish a field threshold voltage,” as dependent claim 50 recites. Although the channel stop region 102 of Figure 3J of Mastroianni is indeed below the oxide isolation region 125 of Figure 3J of Mastroianni, such isolation region is not part of an isolation trench having two areas filled with two dielectric materials. Mastroianni also fails to disclose a field threshold voltage, much less a “field threshold voltage” established by implanted ions, as dependent claim 50 recites. Mastroianni also fails to discuss ion implantation below a trench, much less ion implantation into the substrate and below the first area “to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material” (claim 51) or “to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material” (claim 52).

Accordingly, the subject matter of claims 45, 49-52 and 68-71 is not anticipated by Mastroianni.

H. CLAIMS 45, 49-52 AND 68-71 ARE NOT ANTICIPATED BY CUSTODE ET AL. (U.S. PATENT NO. 4,990,983)

Claims 45, 49-52 and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Custode et al. (U.S. Patent No. 4,990,983) ("Custode"). With reference to Figures 1 and 13 of Custode, the final Office Action states that the claimed first and second dielectric materials read on the field oxide 34 while the claimed ion implanted region comprises regions 13 and 49. (Office Action at 5).

Custode relates to CMOS devices having the field oxide "split or notched to make at least one field oxide region under which a heavily doped (degenerate) region is formed to increase threshold voltages." (Col. 1, lines 29-33). For this, Custode teaches "thin oxide notched regions 11 of thickness t_1 , in conjunction with a heavily doped (degenerate) p+ region 13 in the semiconductor region immediately beneath the notch." (Col. 4, lines 18-22). Custode further notes that substrate 15 is "P- doped and the degenerate region is P+ doped." (Col. 4, lines 22-25).

Custode does not disclose an isolation trench with a first and second areas filled with a first and second dielectric material, or "an ion implanted region" with ions which are "displaced away from" separated active regions, as independent claim 68 recites. Custode discloses a field oxide region under which a heavily doped region is formed to increase threshold voltages. (Col. 1, lines 29-34). As such, a "heavily doped (degenerate) p+ region 13" is formed immediately beneath "thin oxide notched regions 11," which is part of a field oxide 34 (Col. 4, lines 19-23; Figure 13), but which is not part of an isolation trench, much less of an isolation trench having two areas filled with two dielectric materials. Further, while the claimed invention is directed to an ion implanted region as part of a field isolation region, the heavily doped (degenerate) p+ region 13 of Custode is not part of a field isolation region.

Further, Custode is also silent about ion displacement, which is a limitation of claim 68 of “substantially all ions from said ion implanted region being displaced away from said separated active regions.” Custode only mentions that substrate 15 is “P- doped and the degenerate region is P+ doped.” (Col. 4, lines 22-25). Custode also fails to disclose a field threshold voltage, much less a “field threshold voltage” established by implanted ions, as dependent claim 50 recites. Although Custode notes that the heavily doped (degenerate) p+ region is formed “to increase threshold voltage” (col. 1, lines 29-33), the p+ region of Custode is not formed by implanted ions below a first area of an isolation trench comprising two dielectric materials.

Custode also fails to discuss ion implantation below a trench, much less ion implantation into the substrate and below the first area “to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material” (claim 51) or “to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material” (claim 52). Custode only mentions the thickness t_1 of the thin oxide notched regions 11 and the thickness t_2 of the thick field oxide. Custode is silent, however, about ion implantation in a substrate, or about ion implantation below an area of an isolation trench. Again, the “heavily doped (degenerate) p+ region 13” is formed immediately beneath “thin oxide notched regions 11,” which is part of a field oxide 34 (Col. 4, lines 19-23; Figure 13), but which is not part of an isolation trench. Accordingly, the subject matter of claims 45, 49-52 and 68-71 is again not anticipated by Custode and reversal of the rejection of claims 45, 49-52 and 68-71 is respectfully requested.

I. CLAIMS 46, 49-52, 54, 55, 57, 59, 60, 68-71 AND 73-75 ARE
46, 71, 75 NOT ANTICIPATED BY JOO ET AL. (U.S. PATENT NO.
5,841,163)

Claims 46, 49-52, 54, 55, 57, 59, 60, 68-71 and 73-75 stand rejected under 35 U.S.C. § 102 as being anticipated by Joo et al. (U.S. Patent No. 5,841,163) (“Joo”). The final Office Action asserts that the claimed first and second dielectric materials read on the

field oxide layer 65 of Figure 15 of Joo, while the claimed ion implanted region “comprises layer 68.” (Office Action at 5).

Joo relates to integrated circuit structures having wide and narrow channel stop layers which are formed by employing a first and second field insulation layers coupled with a first and second channel stop impurity layers. (Col. 3, lines 38-47). For example, Joo discloses that impurity ions are implanted below the first field oxide layer and are diffused by a thermal process to form a second channel stop impurity layer. (Col. 6, lines 36-50; Figure 15).

Joo does not disclose first and second areas filled with first and second dielectric materials, or an ion implanted region below the second area, or that substantially all ions in the implanted region are displaced away from the separated active regions, as independent claims 68 and 73 recite. Joo teaches a “first channel stop impurity layer 67” formed beneath the second field oxide layer 66 and “a second channel stop impurity layer 68 beneath the first field oxide layer 65.” (Col. 6, lines 1-3; 35-37; Figure 15). In Joo, however, the first and second channel stop impurity layers and the first and second field oxide layers are not part of an isolation trench, much less of an isolation trench filled with first and second dielectric materials, as in the claimed invention.

Joo also fails to disclose implanted ions in a substrate having “a conductivity type the same as the substrate,” as dependent claims 49 and 57 recite, or implanted ions which “establish a field threshold voltage,” as dependent claims 50 and 54 recite. Joo teaches only that “[B]oron (B) is preferably used” as the first and second channel stop impurity ion. (Col. 5, lines 54-56; Col. 6, lines 32-34). Joo is silent, however, about the type of conductivity of the substrate 51, or about ion implanted having “a conductivity type the same as the substrate,” as dependent claims 49 and 57 recite. Joo also fails to disclose a “field threshold voltage” established by implanted ions, as dependent claims 50 and 54 recite.

Joo does not disclose that the first area “also includes said first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom,” as dependent claims 69 and 74 recite. As noted above, Joo teaches “a second channel stop impurity layer 68 beneath the first field oxide layer 65,” and not an isolation trench having a bottom lined with a first dielectric material and filled with a second dielectric material, as dependent claims 69 and 74 recite. Since Joo is silent about any isolation trench, Joo is further silent about ions which are “displaced away from said active regions by a distance at least equal to a sidewall thickness of said first area filled with said first dielectric material,” as independent claim 73 recites. Joo fails to discuss ion implantation below a trench, much less ion implantation into the substrate and below the first area “to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material” (claims 51, 59) or “to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material” (claims 52, 60). Joo refers only to boron implantation below a thick field oxide to form separate channel stop impurity layers of different thicknesses. In fact, Joo does not even provide the dimensions of the first and second channel stop impurity layers. Joo only mentions that “[T]he first channel stop impurity layer is narrower than the first field insulation layer” and that “[T]he second channel stop impurity layer is wider than the second field insulation layer.” (Col. 3, lines 45-47).


Joo also fails to disclose or suggest the ion spacing limitations recited in claims 55 and 56. Joo does not disclose that “the sidewall thickness of said first area filled with said first dielectric material is less than about forty percent the width of the isolation region” (claim 55) or that “the first dielectric material has a sidewall thickness of at least about one hundred angstroms” (claim 56). Accordingly, none of the limitations of the present invention are described or mentioned in Joo and, thus, the present invention is not anticipated under 35 U.S.C. § 102.

IX. CONCLUSION

In conclusion, Appellant respectfully submits that the final rejection of claims 45, 46, 49-52, 54-57, 59, 60 and 68-76 is in error for at least the reasons given above and it should be reversed.

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Respectfully submitted,

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APPENDIX A

✓ 45. The integrated circuit of claim 68 wherein substantially all the ions are displaced from said separated active regions by at least one hundred angstroms.

✓ 46. The integrated circuit of claim 68 wherein said separated active regions include elements of a memory device.

✓ 49. The integrated circuit of claim 68 wherein the implanted ions have a conductivity type the same as the substrate.

✓ 50. The integrated circuit of claim 68 wherein the implanted ions establish a field threshold voltage.

✓ 51. The integrated circuit of claim 68 wherein the ions are implanted into the substrate below said first area filled with said first dielectric material to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material.

✓ 52. The integrated circuit of claim 68 wherein the ions are implanted into the substrate below said first area filled with said first dielectric material to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material.

✓ 54. The memory device of claim 73 wherein the implanted ions establish a field threshold voltage.

✓ 55. The memory device of claim 73 wherein the sidewall thickness of said first area filled with said first dielectric material is less than about forty percent the width of the isolation region.

✓ 56. The memory device of claim 55 wherein the first dielectric material has a sidewall thickness of at least about one hundred angstroms.

✓ 57. The memory device of claim 73 wherein the implanted ions have a conductivity type the same as the substrate.

✓ 59. The memory device of claim 73 wherein the ions are implanted into the substrate below said first area filled with said first dielectric material to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material.

✓ 60. The memory device of claim 73 wherein the ions are implanted into the substrate below said first area filled with said first dielectric material to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material.

✓ 68. An integrated circuit comprising:

a semiconductor substrate including a plurality of active regions;

a field isolation region separating active regions, wherein said field isolation region includes an isolation trench, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls; and

an ion implanted region of said semiconductor substrate below said second area, substantially all ions from said ion implanted region being displaced away from said separated active regions.

✓ 69. The integrated circuit of claim 68 wherein said first area also includes said first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom.

✓ 70. The integrated circuit of claim 68 wherein said ions from said ion implanted region are displaced away from said separated active regions by a distance at least equal to a sidewall thickness of said first area.

✓ 71. The integrated circuit of claim 68 wherein said first dielectric material and said second dielectric material are the same.

✓ 72. The integrated circuit of claim 68 wherein said first dielectric material and said second dielectric material are different.

✓ 73. A memory device comprising:

a semiconductor substrate including a plurality of active regions; and

a field isolation region separating adjacent active regions, said field isolation region including an isolation trench, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls, and an ion

implanted region of said semiconductor substrate below said second area, substantially all ions from said ion implanted region being displaced away from said active regions by a distance at least equal to a sidewall thickness of said first area filled with said first dielectric material.

✓ 74. The memory device of claim 73 wherein said first area also includes said first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom.

✓ 75. The memory device of claim 73 wherein said first dielectric material and said second dielectric material are the same.

✓ 76. The memory device of claim 73 wherein said first dielectric material and said second dielectric material are different.